Amendments to the Claims:

Claims 1-162 (canceled)

163. (currently amended) A chip package comprising:

a silicon substrate;

a die;

an adhesive material joining a backside of said die to said silicon substrate;

a first polymer layer on said silicon substrate, wherein said die is in a first opening in said first polymer layer;

a second ~~first~~ polymer layer on a front side of said die and on said first polymer layer; ~~, a horizontal outside of said die and across an edge of said die, wherein an opening in said first polymer layer exposes a pad of said die; and~~

a first patterned metal layer on said second polymer layer and over said front side of said die and over said first polymer layer, wherein said first patterned metal layer is connected to said die through a second opening in said second polymer layer, and wherein said first patterned metal layer comprises electroplated copper;

a third polymer layer over said first patterned metal layer, over said second polymer layer, over said front side of said die and over said first polymer layer;

a second patterned metal layer on said third polymer layer, over said front side of said die and over said first polymer layer, wherein said second patterned metal layer is connected to said first patterned metal layer through a third opening in said third polymer layer, and wherein said second patterned metal layer comprises electroplated copper;

an insulating layer on said second patterned metal layer, on said third polymer layer, over said front side of said die and over said first polymer layer, wherein a fourth opening in said insulating layer is over a pad of said second patterned metal layer and exposes said pad; and

a solder bump over said pad and directly over said first polymer layer, wherein said solder bump is connected to said pad through said fourth opening.

~~a metallization structure over said first polymer layer, over said pad, over said horizontal outside and across said edge, wherein said metallization structure comprises an electroplated metal, and wherein said metallization structure is connected to said pad through said opening.~~

164. (currently amended) The chip package in claim 163 further comprising a resistor comprising a portion directly over said first polymer layer. ~~, wherein a cavity in said silicon substrate accommodates said die, said adhesive material joining said backside to a bottom of said cavity.~~

165. (currently amended) The chip package in claim 163 further comprising a capacitor comprising a portion directly over said first polymer layer. ~~, wherein said silicon substrate has a top surface with a first region and a second region, said adhesive material joining said backside to said first region, said horizontal outside being over said second region, wherein said first region is substantially coplanar with said second region.~~

166. (currently amended) The chip package in claim 163, wherein said second ~~first~~ polymer layer comprises polyimide.

167. (currently amended) The chip package in claim 163, wherein said second ~~first~~ polymer layer comprises benzocyclobutene (BCB).

168. (currently amended) The chip package in claim 163, wherein said die comprises a first contact point under said second opening and exposed by said second opening, and a second contact point under a fifth opening in said second polymer layer and exposed by said fifth opening, and wherein said first contact point is connected to said second contact point through said first patterned metal layer. ~~further comprising a second polymer layer on said metallization structure.~~

169. (currently amended) The chip package in claim 163, ~~168,~~ wherein said third ~~second~~ polymer layer comprises polyimide.

170. (currently amended) The chip package in claim 163, ~~168,~~ wherein said third ~~second~~ polymer layer comprises benzocyclobutene (BCB).

171. (currently amended) The chip package in claim 163 further comprising a passive device over said second ~~first~~ polymer layer.

172. (currently amended) The chip package in claim 171, wherein said passive device comprises an inductor over said second polymer layer.

173. (currently amended) The chip package in claim 171, wherein said passive device comprises a capacitor over said second polymer layer.

174. (currently amended) The chip package in claim 171, wherein said passive device comprises a resistor over said second polymer layer.

175. (currently amended) The chip package in claim 171, ~~163~~ wherein said passive device comprises a filter over said second polymer layer. ~~further comprising a solder bump on said metallization structure.~~

176. (currently amended) The chip package in claim 163 further comprising an inductor comprising a portion directly over said first polymer layer. ~~further comprising a gold bump on said metallization structure.~~

177. (currently amended) The chip package in claim 163 further comprising a filter comprising a portion directly over said first polymer layer. ~~second polymer layer on said silicon substrate and at said horizontal outside, wherein said first polymer layer is further on said second polymer layer and said metallization structure is further over~~

~~said second polymer layer.~~

178. (currently amended) The chip package in claim 163, wherein said first polymer layer ~~electroplated metal~~ comprises epoxy. ~~copper.~~

179. (currently amended) A chip package comprising:

a silicon substrate;

a die;

an adhesive material joining a backside of said die to said silicon substrate;

a first polymer layer on said silicon substrate, wherein said die is in a first opening in said first polymer layer;

a second ~~first~~ polymer layer on a front side of said die and on said first polymer layer, ~~over a horizontal outside of said die and across an edge of said die,~~ wherein a second ~~first~~ opening in said second ~~first~~ polymer layer is over ~~exposes~~ a first pad of said die and exposes said first pad, and a third ~~second~~ opening in said second ~~first~~ polymer layer is over ~~exposes~~ a second pad of said die and exposes said second pad; and

a patterned metal layer on ~~metallization structure over~~ said second ~~first~~ polymer layer, over said front side of said die and over said first polymer layer, ~~over said first and second pads, over said horizontal outside and across said edge,~~ wherein said patterned metal layer ~~metallization structure~~ comprises ~~an~~ electroplated copper, ~~metal, and~~ wherein said patterned metal layer ~~metallization structure~~ is connected to ~~connects~~ said first and second pads through said ~~first and~~ second and third openings, and wherein said first pad is connected to said second pad through said patterned metal layer.

180. (currently amended) The chip package in claim 179, wherein said first polymer layer comprises epoxy. ~~a cavity in said silicon substrate accommodates said die, said adhesive material joining said backside to a bottom of said cavity.~~

181. (currently amended) The chip package in claim 179 further comprising a capacitor comprising a portion directly over said first polymer layer. ~~, wherein said silicon substrate has a top surface with a first region and a second region, said adhesive material joining said backside to said first region, said horizontal outside being over said second region, wherein said first region is substantially coplanar with said second region.~~

182. (currently amended) The chip package in claim 179, wherein said second ~~first~~ polymer layer comprises polyimide.

183. (currently amended) The chip package in claim 179, wherein said second ~~first~~ polymer layer comprises benzocyclobutene (BCB).

184. (currently amended) The chip package in claim 179 further comprising a third ~~second~~ polymer layer on said patterned metal layer, on said second polymer layer, over said front side of said die and over said first polymer layer. ~~metallization structure.~~

185. (currently amended) The chip package in claim 184, wherein said third ~~second~~ polymer layer comprises polyimide.

186. (currently amended) The chip package in claim 184, wherein said third ~~second~~ polymer layer comprises benzocyclobutene (BCB).

187. (currently amended) The chip package in claim 179, wherein said patterned metal layer ~~metallization structure~~ comprises a ground bus connecting said first and second pads through said ~~first and~~ second and third openings.

188. (currently amended) The chip package in claim 179, wherein said patterned metal layer ~~metallization structure~~ comprises a power bus connecting said first and second

pads through said ~~first and~~ second and third openings.

189. (currently amended) The chip package in claim 179, wherein said patterned metal layer ~~metallization structure~~ comprises a signal trace connecting said first and second pads through said ~~first and~~ second and third openings.

190. (currently amended) The chip package in claim 179 further comprising a passive device over said second ~~first~~ polymer layer.

191. (currently amended) The chip package in claim 190, wherein said passive device comprises an inductor over said second polymer layer.

192. (currently amended) The chip package in claim 190, wherein said passive device comprises a capacitor over said second polymer layer.

193. (currently amended) The chip package in claim 190, wherein said passive device comprises a resistor over said second polymer layer.

194. (currently amended) The chip package in claim 179 further comprising a solder bump directly over said first polymer layer. ~~on said metallization structure.~~

195. (currently amended) The chip package in claim 179 further comprising a gold bump directly over said first polymer layer. ~~on said metallization structure.~~

196. (currently amended) The chip package in claim 179 further comprising an inductor comprising a portion directly over said first polymer layer. ~~, wherein said electroplated metal comprises copper.~~

197. (currently amended) A chip package comprising:

a substrate;

a die;

an adhesive material joining a backside of said die to said substrate;

a first polymer layer on said substrate ~~and at a horizontal outside of said die~~, wherein said die is in a first opening in said first polymer layer; ~~wherein said first polymer layer has a top surface substantially coplanar with a front side of said die;~~

a second polymer layer on ~~said~~ a front side of said die and ~~,~~ on said first polymer layer ~~and across an edge of said die~~, wherein a second ~~first~~ opening in said second polymer layer is over ~~exposes~~ a first pad of said die and exposes said first pad, and a third ~~second~~ opening in said second polymer layer is over ~~exposes~~ a second pad of said die and exposes said second pad; and

a patterned metal layer ~~metallization structure~~ on said second polymer layer, over said front side of said die and over said first polymer layer, ~~over said first and second polymer layers, over said first and second pads and across said edge,~~ wherein said patterned metal layer ~~metallization structure~~ comprises ~~an~~ electroplated copper, ~~metal,~~ and wherein said patterned metal layer ~~metallization structure~~ comprises a ground bus connecting said first and second pads through said ~~first and~~ second and third openings.

198. (currently amended) The chip package in claim 197 further comprising an inductor comprising a portion directly over said first polymer layer. ~~, wherein said electroplated metal comprises copper.~~

199. (currently amended) The chip package in claim 197 further comprising a resistor comprising a portion directly over said first polymer layer. ~~, wherein said substrate comprises silicon.~~

200. (previously presented) The chip package in claim 197, wherein said first polymer layer comprises epoxy.

201. (currently amended) The chip package in claim 197 further comprising a capacitor comprising a portion directly over said first polymer layer. ~~, wherein said~~

~~substrate has a top surface with a first region and a second region, said die adhesive material joining said backside to said first region, said first polymer layer being over said second region, wherein said first region is substantially coplanar with said second region.~~

202. (previously presented) The chip package in claim 197, wherein said second polymer layer comprises polyimide.

203. (currently amended) The chip package in claim 197 further comprising a third polymer layer on said patterned metal layer. ~~metallization structure.~~

204. (previously presented) The chip package in claim 197, wherein said second polymer layer comprises benzocyclobutene (BCB).

205. (currently amended) The chip package in claim 197 further comprising a solder bump directly over said first polymer layer. ~~on said metallization structure.~~

206. (previously presented) The chip package in claim 197 further comprising a passive device over said second polymer layer.

207. (currently amended) The chip package in claim 206, wherein said passive device comprises an inductor over said second polymer layer.

208. (currently amended) The chip package in claim 206, wherein said passive device comprises a capacitor over said second polymer layer.